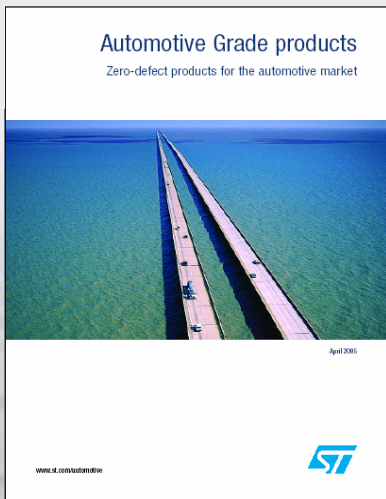


An Industrialization program for DPPM reduction

*A joint presentation of STMicroelectronics and
Test advantage*



*Introduction: An automotive
grade program deployment scheme*

Introduction

Defects do exist. Defects are embedded in the physical properties of materials and potential defectivity in equipments, designs, test programs and test equipments.

Zero failure is achieved by the means of defects reduction activity and robustness validation, detection, screening.

- By reducing the defectivity
- By developing robust electronics and applications to failure modes
- By applying Failure mode driven stress and screening to remove weak parts
- *By effective detection of defects or weak parts before reaching the customer.*

This presentation describe an Industrial program aimed to implement PAT (Parts Average Testing) at Electrical wafer Sort.

Introduction

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ST Automotive Grade

For the last 3 years ST has launched this major effort to improve automotive product quality and to establish new standards. The improvement road map is detailed in our Automotive Grade strategy.

For details on this strategy please refer to the Automotive grade brochure.

This effort requires specific and smart developments across the entire organisation involved with automotive products over the current year with over 2000 products targeted to be “Automotive Grade”.

All ST products benefit from the Industrial efforts developed during the Automotive Grade strategy implementation.



ST Automotive Grade

- The objective to drive toward “Zero Defects” in terms of:
Culture

This is achieved by the means of Automotive Grade Awareness within ST and with its partners.

- Automotive Executive Council and reporting
- Policy deployment and training
- Brochures
- Automotive Grade Product status flag in www.st.com

Performance in Quality & Service

- In order to qualify for Automotive Grade, products are required to respect specific requirements of:
 - Design,
 - Characterisation
 - Qualification
 - Manufacturing processes, detection and screening



Automotive Grade

Key Criteria: ref to ST Internal procedure SOP 2.7.5

- Compliancy to the guidelines of:
 - AEC-Q100 or Q101 (Product Qualification).
AEC Q003 (Product Characterization).
 - AEC Q001 & Q002 (SYA & PAT at ETS).
- Availability of PPAP documents on ST intranet.
- Application of specific manufacturing and process rules.
- Implementation of specific screening and test methods during manufacturing based on sound risk management.



ST Automotive Grade Planning & Deployment

SHORT TERM – SCREEN / STOP DEFECTS

Parallel Activities

**ONGOING & LONG TERM
CONTINUOUS IMPROVEMENT,
PREVENTION**

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An Industrialization program for DPPM reduction

*Detection is a key component of
robust electronic devices processing*



SYA and PAT @ Wafer Sort

- *Standardization of SYA (Statistical Yield Analysis) at EWS as recommended by AEC Q002 guidelines.*
 - SYL (Statistical Yield Limit)
 - SBL (Statistical Bin Limit)
- *Implementation of PAT (Part Average Testing) at Electrical wafer sort as recommended by AEC Q001 guidelines using automatic production analysis and decision maker.*
 - *Adaptive* Dynamic PAT
 - Geographic PAT
 - Wafer Map Stacking



Basis for PAT

- “History has shown that parts with abnormal characteristics significantly contribute to quality and reliability problems.”¹
- Quality is inversely proportional to *variance*
 - Eliminating classified outlier devices from the “Passing Devices” population will reduce the number of early life failures

1. AEC-Component Technical Committee: AEC-Q001-Rev-C



Elements for Comprehensive Outlier Detection

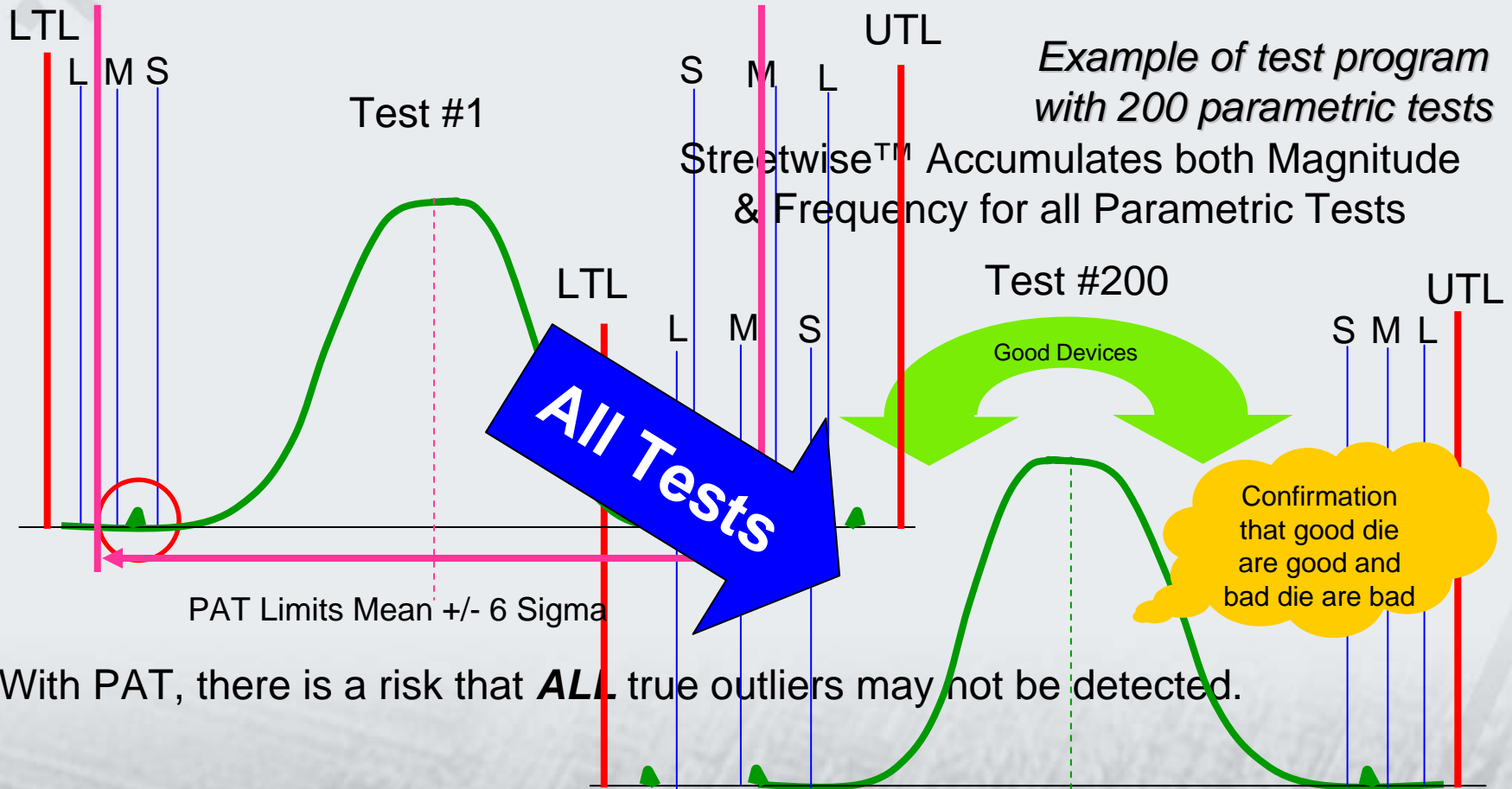
- Utilizes a data analysis engine that identifies “*Variance*” from the data population and defines the magnitude of that variance for a given test.
- Accumulates the frequency of each outlier magnitude occurrence across ALL tests for “qualified” outlier *Device Classification*

Elements for Comprehensive Outlier Detection

- Automatic processing of ALL data distribution types.
- Automatic application of outlier detection algorithms on a per wafer per test basis.
- Operates on ALL parametric tests automatically.
- Comprehension of Test Limits and Asymmetrical data distributions in determining control limit locations.
- Advanced Spatial Outlier Detection
- Ease of setup with revision controlled Recipes.



Confirmation of Device Quality



With PAT, there is a risk that **ALL** true outliers may not be detected.

Device Classification

Rules Managed via Recipe

- Outlier Device Classification using Magnitude and Frequency
- Specific Tests may be considered uniquely

Example Classification Rule:

Critical Device Outlier = $L > 0$ or $M > 3$ or $S > 5$ = **Bin 25**

A device may exhibit a smaller magnitude of variance but have this occurrence across multiple tests confirming a quality risk device

Geographic Analysis Requirements

Comprehend test fail bins and parametric analysis bin results
per *Electrical Wafer Sort Flow*

Flexible recipe defined Spatial Analysis

- Detection of repeating patterns
- **Good** die in **Bad** neighborhood
- Cluster Detection

Proximity Analysis Based on a Specified Bin # or #'s

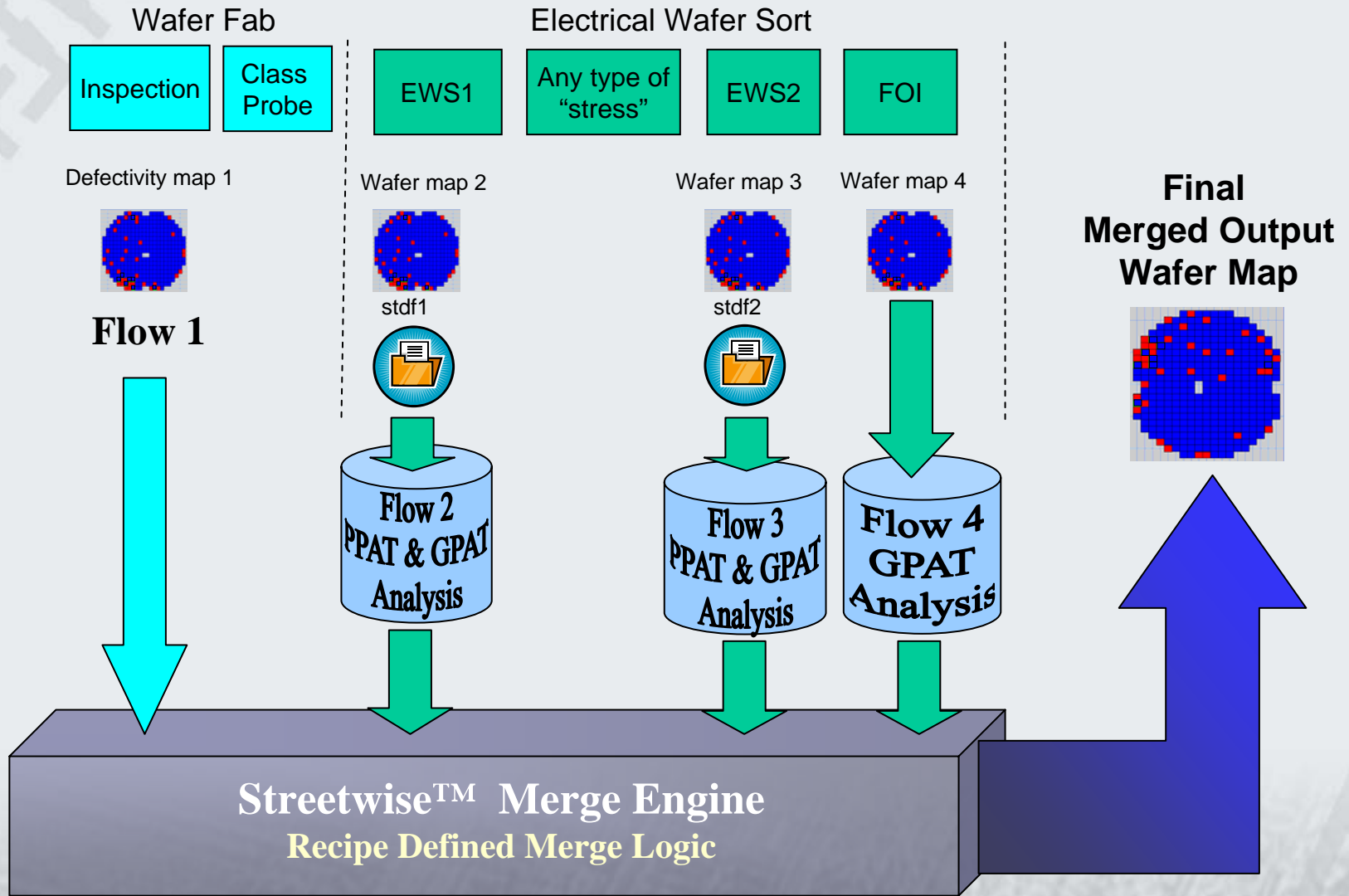
- Wafer edge weighting
- Corner weighting
- Guard banding
- Smoothing

Composite Lot Analysis

- Superimpose lot level wafer maps and perform analysis per X/Y coordinate based on user defined defect density.



Multi-Flow Analysis & Support



An Industrialization program for DPPM reduction

*Definition of a
comprehensive
solution*



A Comprehensive solution requires

- **Data Mgt. Infrastructure**

PAT is not implemented as a local and customized tool but an integral part of the Data mgmt infrastructure . Links with Data files (wafer maps and STDF files repository are mandatory) also links with the manufacturing execution system. (like wafers packing integration)

- **Advanced Outlier Detection**

Adaptive per Wafer per Test analysis in a seamlessly integrated solution supporting multi-flow processing of all test data. Focus on Qualified device classification methodology across all parametric test results for accurate Outlier Detection

- **Risk management in the proposed solution**

The proposed solution driving detection for Zero failure must be mistake proven, potential risk addressed and controlled. (FMEA)



A Comprehensive solution requires

- **Links with product referential**

To allow product engineers to control the product test configuration from remote and related changes (recipe,... steps) links with referential are required.

- **Links with Non conforming lots and MRB management**

Due to introduction of advanced data analysis techniques the risk is generation of non conforming lots. The solution requires exact trace and management of EWS NCL.

- **Training program for engineering, IT and EWS shop floor**

The value of PAT is in the recipe content (exact parameters) and in the exact tool understanding and execution. This required training of all partners in the chain.

An Industrialization program for DPPM reduction

*Data management
infrastructure,
The key elements*



Data management infrastructure

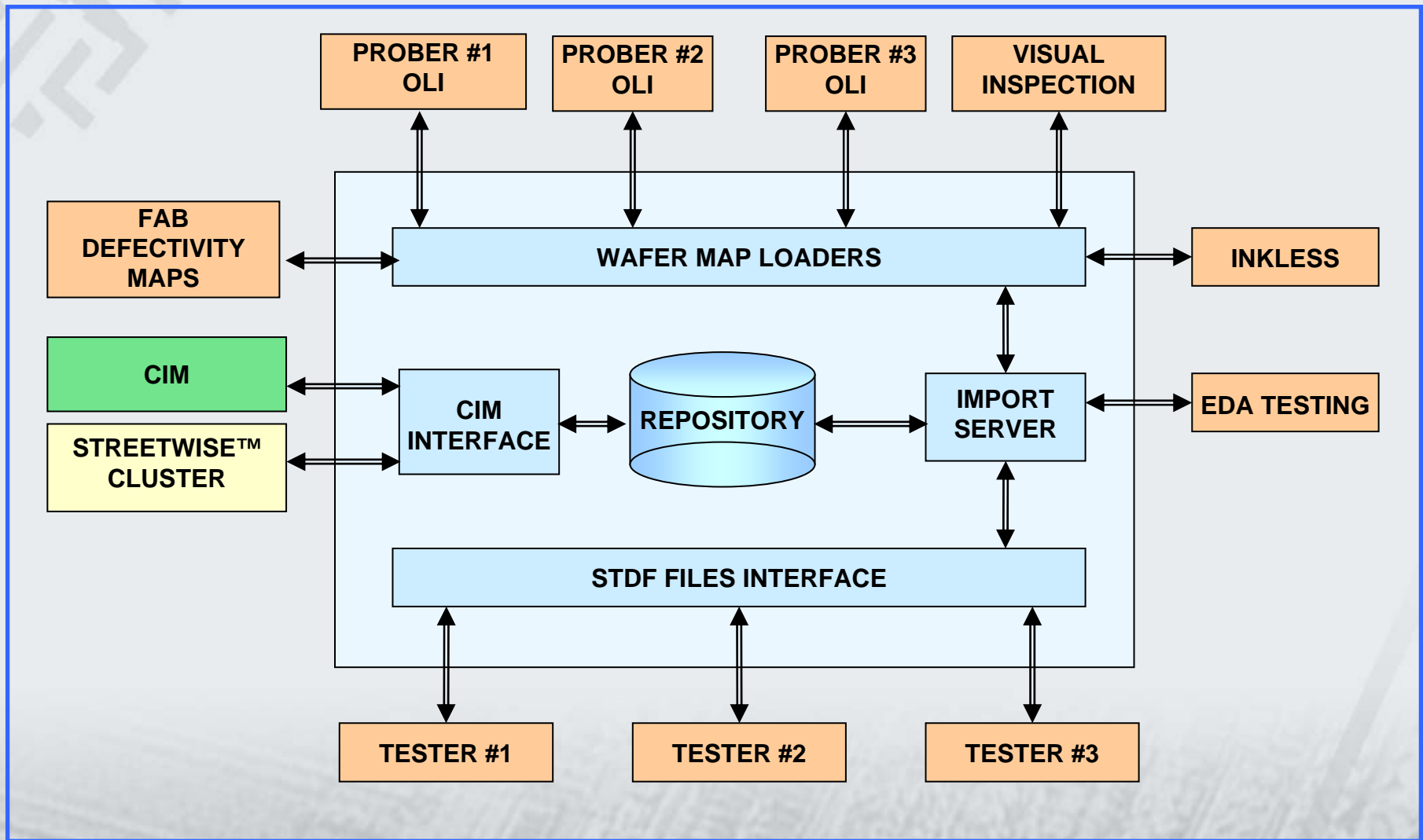
Design criteria

- Focus on Post Electrical Wafer Test
 - Traceability exists
 - Wafer optical number trace is known
 - Dice co-ordinates are known
 - Comprehend per wafer per test data demographic
 - Geographic PAT is possible
 - Immediate response to process and yield enhancement is possible
 - Known Good Dice (KGD) business is fully supported
 - Supports multi-flow data analysis merge
- Use a standard plug-in tool
 - Tool provides data analysis with state of the art adaptive algorithms
 - ST focus on contents, infrastructure, and deployment/training
 - The solution supplier focus on tool implementation and its integration interfaces
- Employ comprehensive multi-criteria analysis
 - Use of real world production test cases

TAI “Streetwise™” was selected as the plug-in solution partner.



Data management infrastructure



Data management infrastructure

Key elements & benefits

- Standard plug-in offered by ST CAM infrastructure for new probers, new testers
 - Speed of introduction of new equipment, Speed of deployment, Flexibility.
- Common WMR Wafer Maps Repository WW for the company
 - Data Integrity, compliancy with infrastructure.
- Compatible with wafer packing mistake proofing (packing, labels, yield control...).
- Does not require to rewrite test programs. Recipe for data elaboration are managed separately for both PAT and SBL.
 - Control and flexibility.
- Integration with the Company CAM system and Electrical Wafer Sort instructions are automatically generated from the company product referential system (Recipes links).
 - Complete product engineering control.

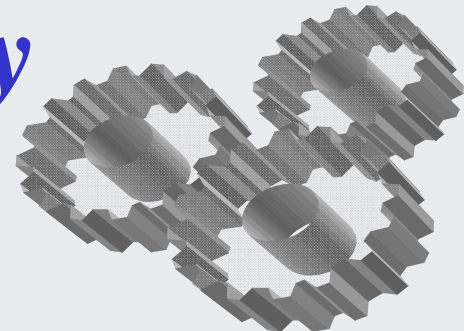


An Industrialization program for DPPM reduction

*Results and summary
Key elements for
success*



Results and summary



Summary

- ST has implemented the Automotive grade program. Most products sold to the Automotive market will be converted this year to the “Qualified” status.
- The Industrial program for DPPM reduction is reaching completion and now in production is the company major wafer level test centers.
- ST and TAI have successfully collaborated in this activity and TAI “Streetwise™” tool integration in ST infrastructure is completed.
- A FMEA study and related control plan are available and a training program for engineering in product divisions and test centers was developed and deployed.
- Product recipes are been established and the production conversion will be completed by Mid 2006. Links with the product referential and CAM systems are established and the operation is under product engineering control.



Results and Summary

Objectives	Expectations	Actual Results
DPPM Reduction	All Mfg. Process Steps to Contribute	PPM Reduction by factor 3.5
Data Mgt Infrastructure	Comprehend all data sources	Achieved
Automation	Fully Automated 24 x 7	Achieved
Data Integrity	Integrity Check	Achieved
Data format Standards	Use SEMI 142 / STDFv4	Achieved
PAT Implementation	PPAT on Critical Tests	PPAT on All Parametric Tests
Deploy Geographic & Stack Analysis	Comprehend only ATE results	Comprehend PPAT, ATE, Defectivity, Visual Results
Yield Mgt. Strategy	Static Analysis Strategy	Per Product Per Flow User Defined Recipe
Minimize Cost (PAT)	< 2% Yield Hit	<0.5% Average Impact
SBL Implementation	Meet AEC Q002	Achieved
SYL Implementation	Meet AEC Q002	Standardized



Key elements for success

- Examine the needs and success conditions in details
- Validate upfront data integrity (STDF)
- Analyze most current STDF and/or Map data per flow
- Analyze the potential risk and define FMEA (control risk elements)
- Do not analyze at the Test program level. Adaptive per Wafer per Test analysis for accurate distribution shapes and location of Control Limits
- Geographical analysis considering PPAT results and Multi-Flow Merge
- Select the best partner after careful trials for data analysis solutions
- Integrate the solution in a solid test infrastructure
- Provide the means to product engineering to simulate and develop appropriate recipe
- Commit and train, execute

